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DE 100 60 436 A 1

Mit Einverständnis des Anmelders offengelegte Anmeldung gemäß § 31 Abs. 2 Ziffer 1 PatG

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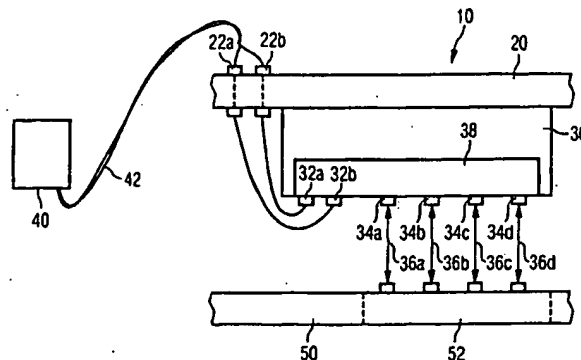
56 Entgegenhaltungen:
DE 37 24 144 A1
JP05-264667AA;

Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen

Prüfungsantrag gem. § 44 PatG ist gestellt

54 Testeinrichtung zum Hochfrequenztest schneller integrierter Schaltkreise

57 Bei einer Testeinrichtung zum Hochfrequenztest schneller integrierter Schaltkreise, insbesondere Halbleiterspeicherbausteine, umfaßt ein auf einem tragenden Element (20; 60) angeordneter Halbleiterschaltkreis (30) erste Anschlüsse (32a, 32b), ausgelegt zur niederfrequenten Signalkommunikation mit einem Testgerät (40), insbesondere zur Aufnahme von niederfrequenten Testsignalen wie Daten-, Steuer-, Adreß- und Taktsignalen, Mittel (38) zum Erzeugen hochfrequenter Testsignale auf Basis eingehender niederfrequenter Testsignale des Testgeräts, und zweite Anschlüsse (34a-34d), ausgelegt zur hochfrequenten Signalkommunikation mit einem zu testenden Schaltkreis (52; 54), insbesondere zur Abgabe der hochfrequenten Testsignale und zur Aufnahme der vom zu testenden Schaltkreis (52; 54) erzeugten Antwortsignale.



DE 100 60 436 A 1

DE10060436

Biblio

Desc

Claims

Page 1

Drawing

**No English title available.**

Patent Number: DE10060436

Publication
date: 2002-03-28Inventor(s): KRAUSE GUNNAR (DE); KUHN JUSTUS (DE); HUEBNER MICHAEL (DE);
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Applicant(s): INFINEON TECHNOLOGIES AG (DE)

Requested
Patent: ☐ DE10060436Application
Number: DE20001060436 20001205Priority
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Classification: G01R31/3181; G11C29/00; G01R31/3177; H01L21/66EC
Classification: G01R31/319C1, G11C29/00B2E, G11C29/00T

Equivalents:

Abstract

Data supplied from the esp@cenet database - l2

t s12/3,ic,ba/all

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DIALOG(R)File 351:Derwent WPI

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015389454

WPI Acc No: 2003-450398/200343

XRAM Acc No: C03-119865

XRPX Acc No: N03-359193

Test device for *high* *frequency* testing of fast integrated circuits has *low* and *high* *frequency* communications connections, arrangement for producing and receiving *high* *frequency* test signals

Patent Assignee: INFINEON TECHNOLOGIES AG (INFN)

Inventor: HUEBNER M; KRAUSE G; KUHN J; MUELLER J; POECHMUELLER P;

WEIDENHOEFER J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 10060436	A1	20020328	DE 1060436	A	20001205	200343 B

Priority Applications (No Type Date): DE 1060436 A 20001205

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10060436	A1		9	G01R-031/3181	

Abstract (Basic): DE 10060436 A1

Abstract (Basic):

NOVELTY - The device has connections for *low* *frequency* or LF signal communications with test equipment, especially for acquiring LF test signals such as data, control, address and clock signals, an arrangement for producing *high* *frequency* or HF test signals based on incoming LF test signals and second connections for HF signal communications with a circuit under test, especially for outputting HF test signals and receiving response signals from the circuit.

DETAILED DESCRIPTION - The device has first connections (32a,32b) for *low* *frequency* signal communications with a test equipment (40), especially for acquiring *low* *frequency* test signals such as data, control, address and clock signals, an arrangement (38) for producing *high* *frequency* test signals based on incoming *low* *frequency* test signals and second connections (34a-34d) for *high* *frequency* signal communications with a circuit under test (54), especially for outputting *high* *frequency* test signals and receiving response signals from the circuit.

USE - For Built Outside *Self*-Test* (BOST) *high* *frequency* testing of fast integrated circuits, especially semiconducting components on component planes (claimed) such as *dynamic* random access *memory* .

ADVANTAGE - Enables testing on wafer planes in a simple, inexpensive manner.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic representation of an inventive arrangement

First connections for *low* *frequency* signal communications (32a,32b)

Test equipment (40)

Arrangement for producing *high* *frequency* test signals (38)

*Best - Try to locate
to provide
info for
Muenchen*

Second connections for *high* *frequency* signal communications
(34a-34d)

Circuit under test (54)

pp; 9 DwgNo 1/5

International Patent Class (Main): G01R-031/3181

International Patent Class (Additional): G01R-031/3177; G11C-029/00;
H01L-021/66

12/3, IC, BA/2

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015021399

WPI Acc No: 2003-081916/200308

XRPX Acc No: N03-064260

Large scale integrated semiconductor device has built-in *self* *test*
circuit that outputs evaluation result to SRAM, after completion of
DRAM test

Patent Assignee: HITACHI LTD (HITA); HITACHI MICON SYSTEM KK (HITA-N)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002298598	A	20021011	JP 200199323	A	20010330	200308 B

Priority Applications (No Type Date): JP 200199323 A 20010330

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002298598	A		19	G11C-029/00	

Abstract (Basic): JP 2002298598 A

Abstract (Basic):

NOVELTY - A built-in *self* *test* (*BIST*) circuit (10) outputs
evaluation signal and fail bit-map information to a SRAM (3) at high
speed, after the test completion of *DRAM* (204).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for
semiconductor device test method.

USE - Large scale integrated semiconductor device.

ADVANTAGE - The fail bit map information stored in the SRAM can be
read by a *low* speed tester. Test *frequency* is enlarged and the
yield and capability of memory are improved.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of
the LSI semiconductor device. (Drawing includes non-English language
text).

SRAM (3)

Built-in *self* *test* circuit (10)

DRAM (204)

pp; 19 DwgNo 2/15

International Patent Class (Main): G11C-029/00

International Patent Class (Additional): G01R-031/28; G01R-031/3183

12/3, IC, BA/3

DIALOG(R) File 351:Derwent WPI

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